This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

Multi-Input Switched-Capacitor Multilevel Inverter for High-Frequency AC Power Distribution

S. Raghu Raman, *Student Member, IEEE,* K.W.E. Cheng, *Senior Member, IEEE,* and Ye Yuanmao, *Member, IEEE*

***Abstract*—This paper proposes a switched-capacitor multilevel inverter for high frequency AC power distribution systems. The proposed topology produces a staircase waveform with higher number of output levels employing fewer components compared to several existing switched capacitor multilevel inverters in the literature. This topology is beneficial where asymmetric DC voltage sources are available e.g. incase of renewable energy farms based AC microgrids and modern electric vehicles. Utilizing the available DC sources as inputs for a single inverter solves the major problem of connecting several inverters in parallel. Additionally, the need to stack voltage sources, like batteries or super-capacitors, in series which demand charge equalization algorithms, are eliminated as the voltage sources employed share a common ground. The inverter inherently solves the problem of capacitor voltage balancing as each capacitor is charged to the value equal to one of input voltage every cycle. State analysis, losses and the selection of capacitance are examined. Simulation and experimental results at different distribution frequencies, power levels and output harmonic content are provided to demonstrate the feasibility of the proposed multilevel inverter topology.**

***Index Terms*—H-bridge, HFAC power distribution, high frequency DC/AC Inverter, multilevel inverter, selective harmonic elimination, switched-capacitor**

I. Introduction

THE significant advantage that High Frequency Alternating Current (HFAC) Power Distribution Systems (PDS) offer over conventional Direct Current (DC) PDS is that HFAC PDS eliminates the need for a rectifier and a filter stage at the front-end power source, and the need for an inverter in the point-of-load power supply [1], [2]. This substantial reduction in the number of power conversion stages results in lower component number, thereby improving reliability and efficiency, while reducing the cost. HFAC PDS aids in reducing the size of passive components which leads to higher power density systems, improves heat distribution and has latent ability to employ connector-less power transfer. Smaller output capacitors improve dynamic response. High-voltage low-current distribution can easily be achieved utilizing compact HF transformers. They also offer the flexibility to cater loads at different voltage levels, provide galvanic isolation and are crucial to realize connector-less power transfer. Switching off a large magnitude of AC when passing through a zero is easier than switching off large DC. Several studies show that frequencies over 10 kHz are safer to human cells and tissues than DC [1]. These exciting features and advantages over DC PDS makes HFAC PDS a promising alternative for future power net.

HFAC PDS architecture includes a front-end HFAC power source, a HF distribution line and point-of-load voltage regulator modules. These systems employ resonant converters to enhance efficiency, power factor and energy density, and alleviate adverse EMI effects [3], [4]. In 1980s, NASA pioneered research on HFAC PDS for its space station. A single-phase system rated at 25 kW with 20 kHz line frequency and $440V_{rms}$ line voltage was implemented successfully [5]. At this frequency, the energy transferred per cycle is lower by 50 times as compared to a 400 Hz system (which also failed to provide efficient and reliable solution [6]). The number of components is reduced by a factor of 5 and power loss by 67% when compared to three-phase systems [1]. Due to the aforementioned benefits, HFAC PDS have been further examined in diverse fields.

A comprehensive review of HFAC PDS for telecommunication, computer and aerospace systems has been presented in [7]. Applications also extend to lighting systems [2], motor drives [8], [9], automotives [10], [11], microgrids [12] and gate drivers [13]. Papers claim and conclude that HFAC scheme solve several hurdles in efficient power delivery. This paper explores switched-capacitor multilevel inverters (SCMLI) as input sources for HFAC PDS.

Proliferation of Multilevel Inverters (MLI) can be attributed to the demand for higher power equipments in the industry and the potential of MLI to gratify industry needs with several attractive traits [14]. With increase in number of voltage levels, the synthesized output waveform has more steps, which profoundly mitigates the harmonic content in the output. MLI are broadly classified into neutral point clamped, capacitor clamped and cascaded types [15]. Unbalanced DC link capacitor voltage and increased component count to obtain higher voltage levels are the major drawbacks for diode clamped (DCI) and capacitor clamped (CCI) types, whereas cascaded H-bridge (CHB) MLI demand relatively higher number of isolated DC voltage sources to obtain higher levels. Several

S. Raghu Raman (raghu.sekhar@connect.polyu.hk) and corresponding author K.W.E Cheng (eeecheng@polyu.edu.hk) are with the Department of Electrical Engineering, The Hong Kong Polytechnic University, Hong Kong. Ye Yuanmao (yuanmao.ye@connect.polyu.hk) is with the School of Automation, Guangdong University of Technology, China.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

topologies of MLI that do not fall into the category of the three aforementioned inverters have also been recently published. Coupled inductor based MLI have been discussed in [16], [17]. The structure is simple but is not feasible to obtain higher levels. An effective topology based on reversing-voltage component is presented in [18]. Topologies of SCMLI published in recent years is reviewed in the next section.

II. Review of Switched-Capacitor Multilevel Inverters

SCMLI have been gaining attention in recent years [19]–[32]. This new family of MLI inherently solves the issue of unbalanced capacitor voltages that afflicts numerous classical topologies. It is also possible to produce higher number of voltage levels while employing a single voltage source unlike cascaded MLI. The common architecture in this family of MLI includes a front-end SC based DC-DC converter that can synthesize multiple levels at the DC bus cascaded with a H-bridge to obtain the corresponding bipolar levels, and a zero level, at the output. Number of output levels can be enhanced by increasing the number of input voltage sources, SC and power switches in the front-end SC DC-DC converter. However, the number of additional components and input voltage sources required to enhance the output voltage level by SCMLI is greatly reduced when compared to the conventional topologies.

SC DC-DC converters offer the advantage to convert input voltage to integral multiple output levels without utilizing inductors. This voltage conversion is accomplished by charging the SCs to input voltage magnitude first (by connecting SC in parallel to source) and later connecting the input voltage source and SCs in series to the load. This simple idea can be extended to generate multiple voltage levels. A cascaded MLI based on SC voltage doubler is proposed in [21], [23]. The same circuitry, without cascade connection, is extended to higher levels in [19], [20]. A novel front-end SC DC-DC converter that can also be extended to higher voltage levels is proposed in [22]. SC based boost MLI was proposed in [28]. It is based on the principle of partial charging of capacitors. However, it is very difficult to control the voltage precisely. Using a single series parallel SC unit, a bi-directional SCMLI is presented in [31]. The common feature in all SCMLI topologies is the back-end H-bridge inverter. Therefore, the key is to design the front-end SC DC-DC converter that can produce multiple levels.

Several Pulse Width Modulation (PWM) techniques have been investigated. Phase shift modulation strategy for HFAC PDS was implemented in [21]. The performance of the multilevel carrier based sinusoidal PWM and SHE with staircase modulation has been evaluated in [22]. It concludes that the latter offers a better trade off as it mitigates the harmonics to an acceptable content and avoids higher transistor switching losses. Level and Phase Shifted PWM was introduced and implemented in [24] and infers that in contrast to level shifted PWM, it empowers the circuit to use a smaller SC, thereby improving the conversion efficiency.

For a given power level, a SCMLI topology has the luxury to employ a smaller capacitor for HFAC applications when compared to 50 Hz / 60 Hz applications. Topologies reviewed employ a single input voltage source to obtain multiple output voltage levels. However, in order to utilize each source under situations where multiple input voltage sources are available, these inverters have to operate either with sources stacked in series or connect inverters employing single input voltage sources in parallel to achieve higher power levels. On one hand, series connection of batteries requires voltage balancing schemes and increase the voltage ratings of semiconductor switches. On the other hand, parallel operation of inverters are challenging and demand advanced control algorithms [32]. This paper, therefore, focuses to explore novel SCMLI topologies with multiple input voltage sources, sharing a common ground, that can be employed in areas like microgrids and electric vehicle networks where asymmetric input sources are available with emphasis on high frequency AC power distribution.

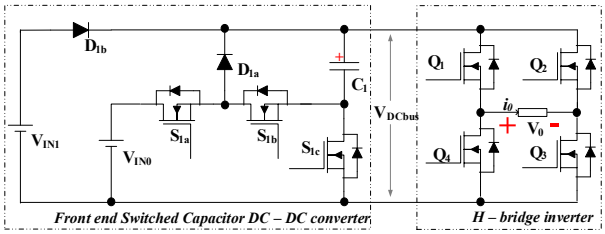


Fig. 1: Proposed 7 level SCMLI topology

III. Proposed Topology and Operating Principle

The proposed 7-level SCMLI, shown in Fig.1, consists of a SC based DC-DC converter which employs two input sources (V_{IN0} and V_{IN1}), three transistors (S_{1a}, S_{1b}, and S_{1c}), two diodes (D_{1a} and D_{1b}) and a capacitor (C_1). DC levels obtained at the inverter DC bus include V_{IN0}, V_{IN1}, $V_{IN0}+V_{IN1}$. The H-bridge inverter employing transistors Q_1 to Q_4 effectively produces 6 bipolar levels and a zero (0, $\pm V_{IN0}$, $\pm V_{IN1}$, $\pm(V_{IN0}+V_{IN1})$) across the load. For primary analysis, it is assumed that the switches and the voltage sources employed are ideal, capacitance is large enough to maintain a constant voltage and supply constant output current, and the voltage ripple across them is small enough to be neglected. Table I explains the switching logic of the proposed inverter. The working states are explained in the following subsections.

A. Output voltage = $\pm V_{IN1}$ state

Capacitor C_1, is charged to the input voltage V_{IN1} through D_{1b} by turning ON transistor S_{1c}. Transistors S_{1a}, S_{1b} and diode D_{1a} remain turned OFF. The DC bus voltage at this state is equal to V_{IN1} as V_{IN0} is blocked by turning OFF transistor S_{1a}. Voltage source V_{IN1} alone supplies power to the load. Fig. 2(a) depicts the equivalent circuit for $V_0 = +V_{IN1}$.

B. Output voltage = $\pm V_{IN0}$ state

For normal operation of the proposed inverter, $V_{IN0} > V_{IN1}$. In the DC - DC converter, only transistor S_{1a} is turned

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

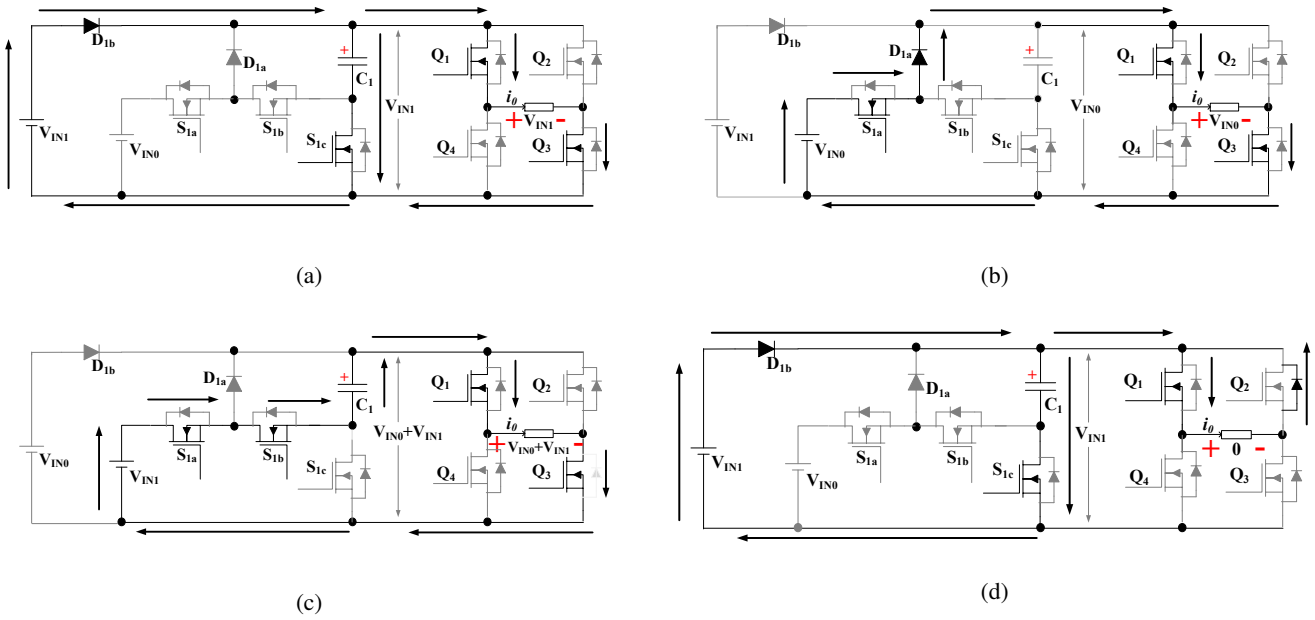


Fig. 2: Equivalent circuits of the 7-level SC MLI to obtain different voltage levels.(a) V_o = V_{IN1} (b) V_o = V_{IN0} (c) V_o = $V_{IN0} + V_{IN1}$ (d) V_o = 0

ON while other transistors are turned OFF. Therefore, V_{IN0} is connected to the DC bus through diode D_{1a}. As $V_{IN0} > V_{IN1}$, diode D_{1b} is reverse biased and hence blocks V_{IN1}. Fig. 2(b) depicts the equivalent circuit for $V_0 = +V_{IN0}$. The capacitor C_1 is open during this state. Therefore, its voltage remains at V_{IN1}.

C. Output voltage = $\pm(V_{IN0} + V_{IN1})$ state

Capacitor C_1, charged to V_{IN1}, is connected in series with input voltage source V_{IN0} by turning ON transistors S_{1a} and S_{1b}. Diode D_{1b} is reverse biased and blocks V_{IN1}. The net voltage that appears across the DC bus now is equal to $V_{IN0}+V_{IN1}$. In this state, input voltage source V_{IN0} and capacitor C_1 supply power to the load. Fig. 2(c) depicts the equivalent circuit for $V_0 = +(V_{IN0} + V_{IN1})$.

D. Output voltage = $0V$ state

To obtain zero level at the output after the positive half cycle(Fig. 2 (d)), only transistor Q_1 is turned ON, while all the other switches in the H-bridge inverter remain turned OFF. The body diode of transistor Q_2 is employed for free-wheeling. Similarly, to obtain zero level at the output after the negative half cycle, only transistor Q_4 is turned ON, while all the other switches in the full bridge inverter remain turned OFF. In this case, the body diode of transitor Q_3 is employed for free-wheeling. The switches in the front-end converter remain in their previous states.

The operational waveforms for the proposed 7 level inverter are shown in Fig. 3. Using these waveforms, it is possible to further comprehend the working states of the SCMLI. If V_{IN0} = $48V$ and V_{IN1} = $24V$, the output voltage waveform would have 0, $\pm 24V$, $\pm 48V$ and $\pm 72V$. The voltage across the capacitor C_1, would always be constant at 24 V.

TABLE I: Switching logic for the 7-level SCMLI

S_{1a}	S_{1b}	S_{1c}	Q_1	Q_2	Q_3	Q_4	V_0
0	0	1	1	0	1	0	V_{IN_1}
1	0	0	1	0	1	0	V_{IN_0}
1	1	0	1	0	1	0	$V_{IN_0} + V_{IN_1}$
0	0	1	1	0	0	0	0
0	0	1	0	1	0	1	- V_{IN_1}
1	0	0	0	1	0	1	- V_{IN_2}
1	1	0	0	1	0	1	- $(V_{IN_0} + V_{IN_1})$
0	0	1	0	0	0	1	0

E. Enhancement in voltage levels

To further enhance the number of output levels, additional input voltage sources, capacitors and switches have to be employed. A generalized SCMLI derived from the proposed 7 level inverter is shown in Fig. 4. For example, if $V_{IN0} = 40V$, $V_{IN1} = 20V$ and $V_{IN2} = 10V$, using the switching logic in Table II, an output voltage staircase waveform with values 0, $\pm 10V$, $\pm 20V$,.....,$\pm 70V$ can be obtained. In this case, C_1 and C_2 will be charged to 20 V and 10 V respectively. Basic unit required to realize the 15 level inverter from 7 level inverter is demarcated using dotted lines. Similarly, if the highlighted unit is added to 15-level inverter, a 31 level inverter can be realized. The maximum voltage across the DC bus increases by adding additional input voltage sources. However, optimum number of sources must be added such that the DC bus voltage is within permissible limit and does not induce very high voltage stress to the H-bridge transistors. Number of individual components in SCMLI can be represented w.r.t the number of input voltage sources. If the number of individual input voltage sources employed in the MLI is denoted by 'i', then the number of

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

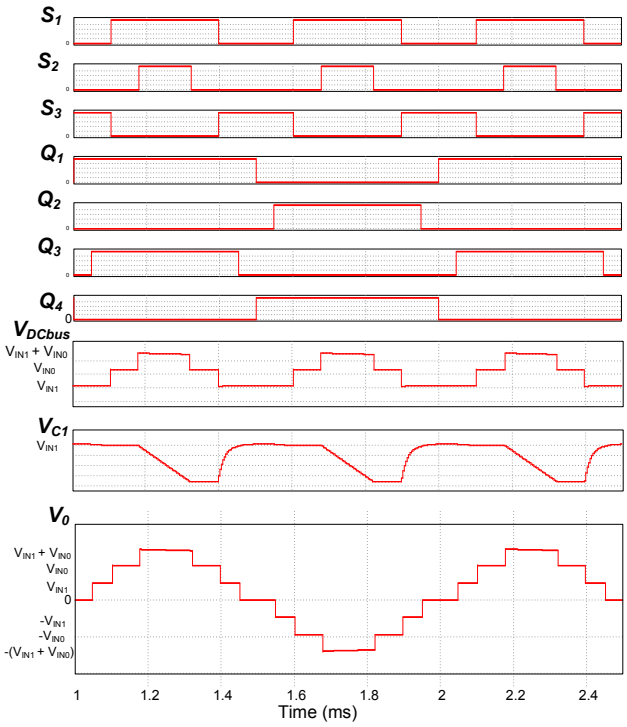


Fig. 3: Operational waveforms of the inverter

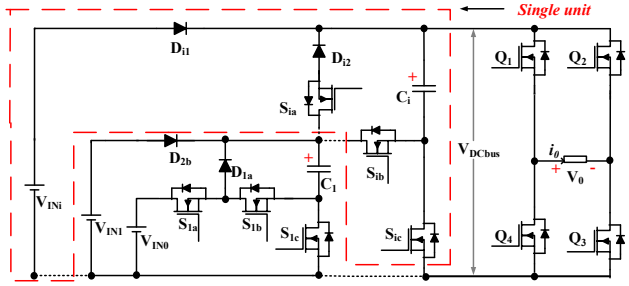


Fig. 4: Generalized topology of the proposed SCMLI

output levels (n_l), number of SCs (n),number of transistors (n_T) and their gate drivers (n_{gd}), number of diodes (n_D) are given by (1) to (4) respectively.

$$n_l = 2^{i+1} - 1 \tag{1}$$

$$n = i - 1 \tag{2}$$

$$n_T = n_{gd} = 3i + 1 \tag{3}$$

$$n_D = 2(i - 1) \tag{4}$$

Eqns. (1) to (4) can be verified using the proposed 15 level inverter shown in Fig. 4. SCMLI topology with higher number of voltage levels without employing additional voltage sources is presented in [29]. It employs a SC based voltage doubler at one of the asymmetric voltage sources (V_{IN1}) to realize two voltage levels from a single source. [30] proposes a seven level inverter employing two unequal voltage sources limited to low voltage and low power applications.

TABLE II: Switching logic to realize a 15-level SCMLI from the generalized topology

S_{1a}	S_{1b}	S_{1c}	S_{2a}	S_{2b}	S_{2c}	V_{DCBUS}
0	0	0	0	0	1	V_{IN_2}
0	0	1	1	0	0	V_{IN_1}
0	0	1	1	1	0	$V_{IN_2} + V_{IN_1}$
1	0	0	1	0	0	V_{IN_0}
1	0	0	1	1	0	$V_{IN_0} + V_{IN_2}$
1	1	0	1	0	0	$V_{IN_0} + V_{IN_1}$
1	1	0	1	1	0	$V_{IN_0} + V_{IN_1} + V_{IN_2}$

IV. Modulation for the Proposed Inverter

Selective Harmonic Elimination (SHE) [33] is a popular technique which eliminates specific harmonics in the output. For Fourier analysis, consider an 'm' level staircase waveform as shown in Fig. 5. With co-efficients a_0 and a_n being equal to zero, applying half and quarter wave symmetry, the waveform can be mathematically represented as:

$$\begin{aligned} v(\omega t) &= \sum_{x=1,3,5} \left(\frac{8}{T} \int_0^{T/4} f(\omega t) sin(x\omega t) d\omega t \right) sin(x\omega t) \\ &= \sum_{x=1,3,5} \frac{4V_{IN}}{x\pi} \{ cosx\theta_1 + ... + cosx\theta_z \} sin(x\omega t) \end{aligned} \tag{5}$$

where, $z = (m-1)/2$ and θ_1 to θ_z are the conducting angles. The fundamental voltage in terms of switching angles is given by:

$$v_1(\omega t) = \frac{4V_{IN}}{\pi} \{ cos\theta_1 + ... + cos\theta_z \} sin(\omega t) \tag{6}$$

The maximum value of fundamental amplitude (V_{1p}) is obtained when the all the switching angles are equal to zero.

$$V_{1p} = \frac{4z}{\pi} V_{IN} \tag{7}$$

SHE computes conduction angles for a given modulation index to eliminate specific harmonics. For example, in a 7 level inverter, only a maximum of two harmonics can be eliminated. Modulation index (M_I) is defined as the ratio of the desired fundamental voltage (V_1) to the maximum obtainable fundamental voltage.

$$M_I = \frac{V_1}{V_{1p}} = \frac{\pi V_1}{4z V_{IN_1}} \tag{8}$$

The harmonic equations to eliminate 5^{th} and 7^{th} harmonic for the proposed seven level SCMLI are given as follows.

$$\begin{cases} cos\theta_1 + cos\theta_2 + cos\theta_3 = 3M_I \\ cos5\theta_1 + cos5\theta_2 + cos5\theta_3 = 0 \\ cos7\theta_1 + cos7\theta_2 + cos7\theta_3 = 0 \end{cases} \tag{9}$$

where,

$$0 < \theta_1 < \theta_2 < \theta_3 < \frac{\pi}{2} \tag{10}$$

For $M_I = 0.84$, the angles, in degrees, computed using selective harmonic elimination are : θ_1 = 15.6°, θ_2 = 18.7°

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

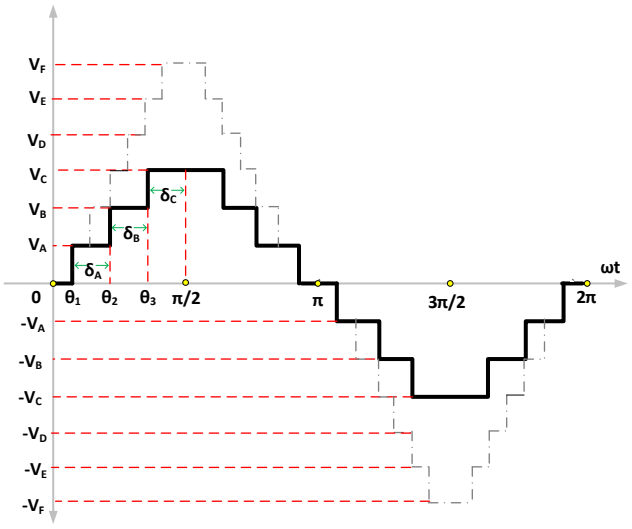


Fig. 5: Generalized staircase and 7 level ideal output voltage waveform

and θ_3 = 52.4°. With 5^{th} and 7^{th} harmonics eliminated, total harmonic distortion (THD) can be given by:

$$T.H.D = \sqrt{\left(\frac{V_{rms}}{V_{1rms}}\right)^2 - 1} = \sqrt{\sum_{n=3,9,11,13..}^{\infty} \left(\frac{V_n}{V_{1rms}}\right)^2} \tag{11}$$

V. Circuit Characteristics and Analysis

For analysis, it is assumed that all transistors are identical with equal on-state resistances (R_{dsON}), the internal resistances (R_{in}) of the voltage sources are equal and the forward voltage drop (V_F) both the diodes are the same. For the proposed SCMLI with i-input voltage sources, n_l voltage levels can be produced (1). Under ideal case, each staircase voltage level ($V_A, V_B, ...$) and capacitor voltage (V_{C_i}) can be expressed using the following set of generalized equations:

$$\begin{cases} V_A = V_{IN_i} \\ V_B = V_{IN_{i-1}} \\ V_C = V_{IN_i} + V_{IN_{i-1}} \\ V_D = V_{IN_{i-2}} \\ V_E = V_{IN_{i-2}} + V_{IN_i} \\ V_F = V_{IN_{i-2}} + V_{IN_{i-1}} \\ ... \\ ... \\ V_U = V_{IN_i} + V_{IN_{i-1}} + ... + V_{IN_0} \\ V_{C_i} = V_{IN_i} \end{cases} \tag{12}$$

General expression for RMS value of the m-level staircase waveform is given by:

$$V_{0_{RMS}} = \sqrt{\frac{2}{\pi}\left(V_A^2\delta_A + V_B^2\delta_B + ... + V_N^2\delta_N\right)} \tag{13}$$

Output waveform is symmetric when the magnitude of input voltage sources are integral multiples of magnitude of the least value of input voltage source. That is, for a seven level output if $V_{IN0} = kV_{IN1}$, where k is a greater than 1. Then, V_{0RMS} of the seven level waveform shown in Fig. 5 is:

$$V_{0_{RMS}} = V_{IN_1}\sqrt{\frac{2}{\pi}(\delta_A + k^2\delta_B + (k+1)^2\delta_C)} \tag{14}$$

Considering non-idealities R_{in}, V_F, R_{dsON} and ESR of the SC, each voltage step and the V_{C1} of the seven level inverter can be represented as –

$$\begin{cases} V_A = V_{IN_1} - V_F - I_o(2R_{ds_{ON}} + R_{in}) \\ V_B = kV_{IN_1} - V_F - I_o(3R_{ds_{ON}} + R_{in}) \\ V_C = kV_{IN_1} + V_{C1} - I_o(4R_{ds_{ON}} + R_{in} + ESR) \\ V_{C1} = V_{IN_1} - V_F - I_{c1}(R_{ds_{ON}} + R_{in} + ESR) \end{cases} \tag{15}$$

where, I_o is the average output current of the front-end converter and I_{c1} is the average capacitor charging current. Eqn. (15) suggests to choose transistors with low R_{dsON}, diodes with V_F and low ESR capacitors for better utilization of available voltage source and improved efficiency.

A. Switched-capacitor analysis

SC is the solitary energy storage element for the proposed SCMLI. It is, therefore, imperative to select the appropriate value of capacitance for the application. The value of the capacitance usually depends on the frequency of operation, maximum load current requirement and the upper limit imposed on the ripple voltage. Under ideal conditions, for the proposed SCMLI topology, during every half cycle the capacitor C_1 is charged to V_{IN1} when connected in parallel to the source and discharged to the load when connected in series with V_{IN0}, as explained in Fig. 2. Considering ideal conditions, C_1 is charged to V_{IN1} during $V_0 = \pm V_{IN1}$ and $V_0 = 0V$ states and discharged only during $V_0 = \pm(V_{IN0} + V_{IN1})$ state. However, in reality the output voltage levels are lower than the input voltages as explained in (15).

The discharging of C_1 is initiated only when switches S_{1a} and S_{1b} of the front-end SC DC-DC converter are turned ON. The discharging period ends when both are turned OFF. During discharging, C_1 along with V_{IN1} supply energy to the load. If the maximum load current is known, this discharging period can be used to determine the optimum value of SC for a given voltage ripple limit. If Q_C is the amount of charge released by C_1 during the period then

$$Q_C = \int_{t_{d1}}^{t_{d2}} I_0 sin(2\pi f_s t - \phi)dt \tag{16}$$

where, the limits t_{d1} and t_{d2} correspond to the discharging period, I_0 is the maximum value of output current ($i_0(t)$), f_s is the fundamental frequency and ϕ is the phase difference between the voltage and current. Ripple voltage (ΔV_C) can be calculated using the angles computed by SHE using

$$\Delta V_C = \frac{1}{2\pi f_s C}\int_{\theta_i}^{\pi-\theta_i} I_0 sin(2\pi f_s t - \phi)d\omega t \tag{17}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

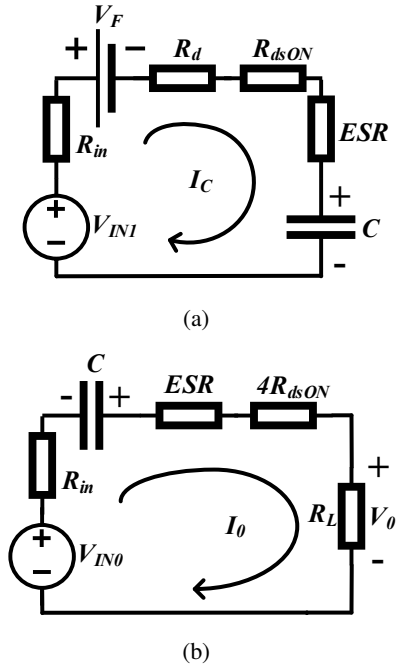


Fig. 6: Equivalent circuits of seven level SCMLI during (a) capacitor charging (b) capacitor discharging

where, θ_i is the angle at which the capacitor starts to discharge and $\pi - \theta_i$ is the angle at which the discharging stops. If p(%) is the limit imposed on the ripple voltage (ΔV_C), then C can be chosen based on the following equation.

$$C \geq \frac{Q_C}{pV_{IN1}} \tag{18}$$

Voltage rating of a capacitor also plays a vital role. In general, as the value of capacitance increases, the physical dimensions of the capacitor also increase which makes the converter bulky. Therefore, it is important to choose an optimum value of capacitance considering all the aforementioned parameters. Most manufacturers' datasheet provide dissipation factor (DF) as a measure of performance. DF, in simple terms is the ratio of energy loss to the energy stored in a capacitor. Assuming, zero parasitic inductance, ESR of an electrolytic capacitor in terms of DF is given by

$$ESR = \frac{DF}{2\pi f_s C} \tag{19}$$

where $DF = tan\delta$, δ is the loss angle between capacitor's impedance vector and the negative reactance axis. Lower DF is a measure of superior quality among capacitors when similar di-electric materials are employed. It is therefore recommended to choose a large enough SC to minimize ESR. Lower ESR reduces voltage drop and conduction loss.

B. Loss Analysis

1) Conduction Loss: In the SC, it is due to power dissipation in the ESR. In the proposed 7 level SCMLI, capacitor C_1 is charged close to V_{IN1} when only S_{1c} is turned ON. The energy stored is discharged to the load when S_{1a} and S_{1c} are turned ON keeping S_{1b} OFF. The maximum capacitor charging current ($I_{C_{ch(m)}}$), deduced from Fig. 6 (a), is given by

$$I_{C_{ch(m)}} = \frac{V_{IN1} - V_F - V_{ci}}{R_d + R_{in} + ESR + R_{ds_{ON}}} = \frac{V_{eq}}{R_{eq}} \tag{20}$$

where, V_{ci} is the initial capacitor voltage, $V_{eq} = V_{IN1} - V_F - V_{ci}$ and $R_{eq} = R_d + R_{in} + ESR + R_{dsON}$. When the difference between V_{IN1} and the initial capacitor voltage (V_{ci}) is lower, $I_{C_{CH(M)}}$ is also reduced. This helps to mitigate spiky current waveforms. Therefore, a large enough capacitor must be chosen to reduce undesired peak currents. Smooth waveforms during charging prolong the life of the SC. The charging characteristic of the capacitor can be represented as

$$i_{C_{ch}}(t) = I_{C_{ch(m)}} e^{t/R_{eq}C} \tag{21}$$

where t is charging time. In the 7 level SCMLI, C_1 is charged twice every cycle. If charging duration $\Delta t = t_2 - t_1$, $I_{C_{chRMS}}$ is given by

$$I_{C_{chRMS}} = \sqrt{\frac{2}{T}\int_{t_1}^{t_2} i^2_{C_{ch}}(t)dt} \tag{22}$$

The conduction loss during charging of C for the 7 level SCMLI can be given as

$$P_{con(ch)} = I^2_{C_{chRMS}} ESR \tag{23}$$

When several SCs are employed, their respective charging currents are utilized to determine the conduction loss. When the capacitor is discharging, its current is equal to the output current. The RMS value of the output current for a purely resistive load is given by

$$I_{C_{disRMS}} = I_{0_{RMS}} = \frac{1}{R_L}\sqrt{\frac{2}{\pi}\left(V_A^2\delta_1 + V_B^2\delta_2 + V_C^2\delta_3\right)} \tag{24}$$

where, V_A, V_B and V_C are given by (12). The conduction loss during discharging is given by

$$P_{con(dis)} = I^2_{0_{RMS}} ESR \tag{25}$$

Conduction loss in the transistors is due to the heat dissipated in R_{dsON} during current flow. Similarly, diode resistance R_d also results in conduction loss. Therefore, it is important to choose components with low internal resistances to boost operating efficiency. The net conduction loss in transistor ($P_{con(T)}$) and diode ($P_{con(D)}$) are given by

$$P_{con(T)} = \sum_{i=1}^{n_T} I^2_{T_i RMS} R_{ds_{ON}} \tag{26}$$

$$P_{con(D)} = \sum_{i=1}^{n_D} I^2_{D_i RMS} R_d \tag{27}$$

2) Switching Loss: It is due to repeated charging and discharging of parasitic capacitance (C_T) in the transistors. C_T is charged to V_T when the transistor is turned OFF and discharges when the transistor turns ON. This leads to overlapping of transistor's voltage and current waveform twice every cycle causing energy loss. For analysis, assume turn-on

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

and turn-off overlapping times are equal (T_{ov}), voltage and current have linear relationships as below.

$$i(t) = I_{Ton}(1 - \frac{t}{T_{ov}}) \tag{28}$$

$$v(t) = V_T \frac{t}{T_{ov}} \tag{29}$$

For every switching cycle, two overlapping – one during transistor turn-on and one during turn-off occur. Then, power loss per transistor during the overlapping period is given by

$$P_{sw(Ton)} = f_s \int_0^{T_{ov}} v(t)i(t) = \frac{V_T I_{Ton} f_s T_{ov}}{6} \tag{30}$$

Similarly, switching loss during turn-off is given by.

$$P_{sw(Toff)} = \frac{V_T I_{Toff} f_s T_{ov}}{6} \tag{31}$$

where, I_{Toff} is the current through the transistor before turn OFF. Switching loss in diodes is due to the reverse recovery [34] is given by

$$P_{sw(D)} = \frac{V_D I_{rrp} f_s t_r}{6} \tag{32}$$

where, t_r is the time taken by the reverse recovery current to fall from its peak value of I_{rrp} to zero when a voltage of V_D is applied across the diode. Efficiency can be calculated by:

$$\eta_{eff} = 1 - \frac{P_L}{P_{in}} \tag{33}$$

where P_{in} is the input power and P_L is the total power loss.

VI. Comparison with conventional multilevel inverter and other SCMLI topologies

Proposed SCMLI has several advantages over conventional topologies. Diode clamped MLI demands a high voltage rating for the blocking diodes. As the number of levels increases, the number of diodes makes the inverter impossible to be implemented. Also, since the voltage at the capacitor terminals are different, the capacitors are discharged to a different values which results in the voltage unbalance problem. These problems is overcome in the proposed SCMLI. DCI obtains $(2n + 3)$ levels for n capacitors used. However, the proposed SCMLI produces $(2^{(n+2)} - 1)$ levels.

Similarly, capacitor clamped MLI requires a large number of storage capacitors when the required number of levels is high. Therefore, this feature makes it very expensive and difficult for package with bulky storage capacitors. For e.g., to realize a 11-level inverter, CCI requires 10 capacitors whereas the proposed SCMLI can realize fifteen levels with only three capacitors. CCI also requires higher number of diodes in comparison to the proposed inverter. Similar to DCI, CCI also has the unbalance capacitor voltages issue.

The major drawback of the cascaded H-bridge (CHB) inverter is the need for separate isolated DC sources. Also, higher number of transistors used in the circuitry increases the cost and size of the inverter. In comparison, the proposed SCMLI uses fewer transistors to obtain a given number of levels. For e.g., CHB requires seven separate DC sources and twenty eight transistors (seven H-bridges) to realize a 15-level inverter whereas the proposed SCMLI only requires three sources, ten transistors and four diodes.

For comparison with other SCMLI topologies using series-parallel SC structures with H-bridge at the back end, the number of SCs (n) is chosen as the reference as most topologies employ a single voltage source. Table III. compares different SCMLI topologies w.r.t to the number of transistors, diodes and voltage sources employed. It is seen that the number of output voltage levels increase exponentially with additional SCs and input voltage sources. However, other topologies have a linear relationship between the number of SCs and the output voltage levels. The voltage stress on the H-bridge transistors the capability to drive inductive loads is limited similar to most topologies. The phase difference between the output voltage and current cannot be greater than $\phi = \theta_1$. To accomodate larger inductive loads, the proposed SCMLI can be operated at lower modulation indices.

The conventional Fibonacci SC DC-AC inverters shown in Fig. 1 of [27] employs more components than the novel inverter proposed in Fig. 2 of [27]. To realize a 15 level (7 x step up) staircase waveform, the conventional SC DC-AC converter employs sixteen SC and sixty two transistors where as novel Fibonacci inverter employs eight SC, twenty four transistors and six diodes. In comparison, the proposed SCMLI requires only two SC, ten transistors and four diodes. However, it employs three unequal voltage sources.

Operating efficiency of any power converter depends on a variety of parameters. Assuming the same quality of components employed, same PWM strategy, similar operating conditions and cooling arrangements, the comparison of efficiency is carried out with respect to the number of components employed for a given number of stepped output voltage levels.

In Table III, the number of components employed in the proposed converter is compared with other SCMLI with H-bridge topologies. Topology from [25] employs the minimum number of switches (transistors+diodes). Therefore, it is compared with the proposed topology with the same simulation parameters as shown in section VII. For the topology from [25], input voltage was fixed at 20 V to mimic the 60 V output peak characteristic, similar to the proposed topology. Two cases of the proposed inverter were considered. In the first case, a DC - DC conversion stage is employed to obtain the desired value of the input voltages. In the second case, the DC - DC conversion stage wasn't employed. Under both scenarios, the proposed inverter offered better efficiency at higher power levels. At lower power levels, the topology from [25] offered better efficiency. This is primarily because of the number of SCs employed by each topology. In [25], two SCs are used to obtain a seven level output whereas the proposed topology uses only one. Due to the higher voltage ripple effect of SCs, the efficiency of topology from [25] is lower. Another reason is that the proposed topology uses SC voltage to output just two out of seven levels and the remaining levels are directly supported by the DC sources; whereas the topology from [25] uses the SC voltage to output five out of seven levels. This reduces the voltage ripple for the proposed topology enabling it to employ smaller SCs helping to save cost and space.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

TABLE III: Comparison of series parallel based SCMLI topologies with H-bridge

	n_T	n_D	i	n_l	H-bridge stress
Fig. 2 [20]	$3n+3$	n	1	$2n+3$	$(n+1)V_c$
Fig. 1 [21]	$6n$	n	n	$4n+1$	nV_{IN}
Fig. 1 [22]	$n+5$	$2n$	1	$2n+3$	$(n+1)V_c$
Fig. 3 [23]	$2n+4$	n	1	$2n+3$	$(n+1)V_c$
Fig. 1 [25]	$3n+4$	0	1	$2n+3$	$(n+1)V_c$
Fig. 2 [26]	$4n+1$	n	1	$4n+1$	nV_{in}
Proposed	$3n+4$	$2n$	$n+1$	$2^{(n+2)}-1$	$\sum V_{ci}$+V_{IN_0}

TABLE IV: Harmonic content in the seven level output voltage waveform

Harmonic	Fundamental	3^{rd}	5^{th}	7^{th}	9^{th}	11^{th}	13^{th}
Simulation (V)	62	3.5	0.1	0.1	5.85	5.95	1.26
Measured (V)	60	3	1	1	6	7	2

In order to increase the efficiency, higher value of SCs can be employed as it proportionately reduces the voltage ripple. However, loss due to ESR, space and cost factors have to be considered. Also, as the number of levels increases, the stress on the voltage H-bridge inverter increases; a common feature to all H-bridge SCMLI topologies reviewed.

The proposed inverter is limited to operate only when there are multiple unequal voltage sources employed. If only a single voltage source is available, it is still possible to generate another voltage level using a switched-capacitor doubler or switched-capacitor based half circuit.

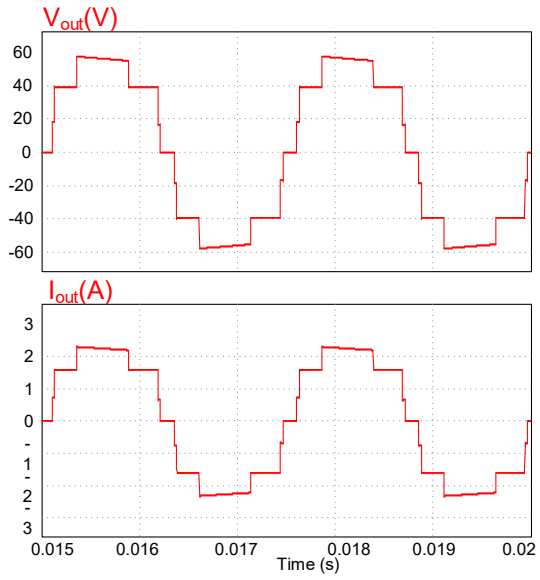
VII. Simulation and Experimental Results

Simulation of proposed SCMLI rated with $V_{IN0} = 40V$, $V_{IN1} = 20V$ employing a $470\mu F$ SC is done. $R_{in} = 0.1\Omega$, ESR = $0.1\Omega, V_F = 0.42V, R_d = 10m\Omega$, $R_{dsON} = 9m\Omega$, θ_1 = 15.6°, θ_2 = 18.7° and θ_3 = 52.4° are considered for simulation. Fig. 7 (a) shows the 7-level staircase output voltage and current operating at 400 Hz when a resistive load of 25 Ω is connected. With increase in power levels, the amplitude of the staircase waveform reduces as the capacitor discharges to a lower value each cycle. The capacitor charging and discharging characteristics are shown in Fig. 7(b). It can be clearly seen that the capacitor charges and discharges twice each cycle. The capacitor charges to V_{c1} as explained in (15) and discharges to a voltage value that is dependent on the load current. Table IV shows the dominant harmonics in the output.

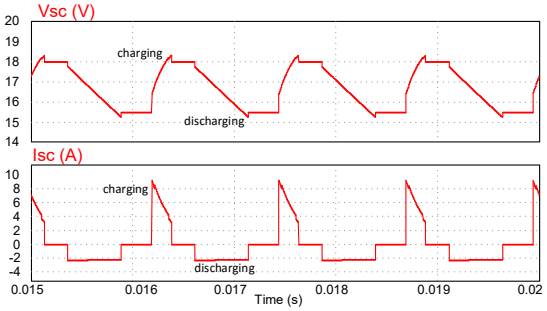
TABLE V: Experiment specifications and components list

Input voltage (V_{IN0})	40 V
Input voltage (V_{IN1})	20 V
Output frequency (f_S)	$\geq$ 400 Hz
Switched-capacitor (C_1)	470 μF
Transistors (N-channel MOSFETs)	FDB3632
Diodes (Schottky Rectifier)	NTST30U100CT
Maximum power	250 W
Controller	TMS320F28335
Gate Drivers	IR2113

Table V details the experiment specifications and the components employed. A simple algorithm is developed on



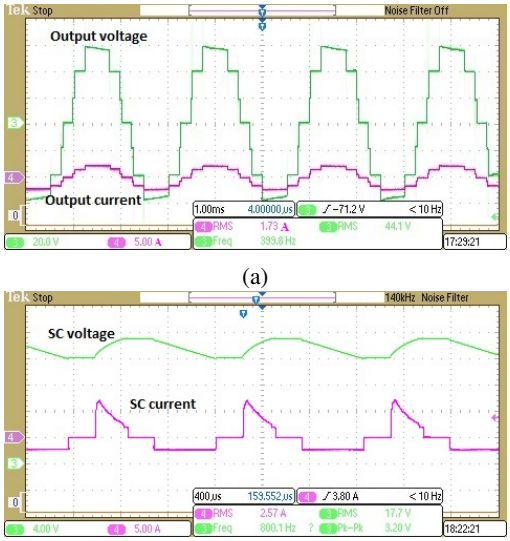
(a)



(b)

Fig. 7: Simulation waveforms at 400 Hz including non-idealities : (a) output voltage and current (b) switched capacitor voltage and current

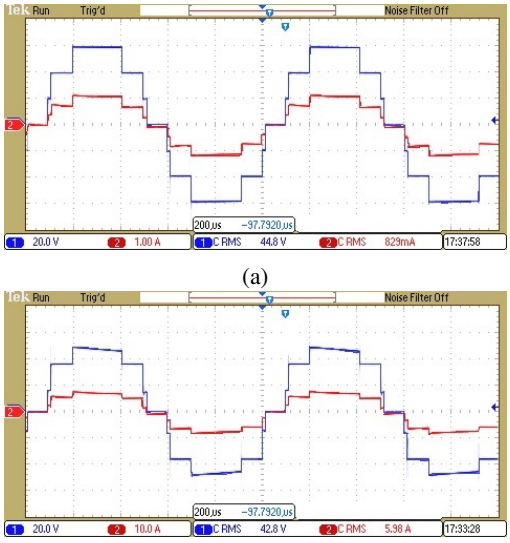
This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics



(a)

(b)

Fig. 8: Measured 400 Hz waveforms (a) Output voltage and current (b) Switched capacitor voltage and current



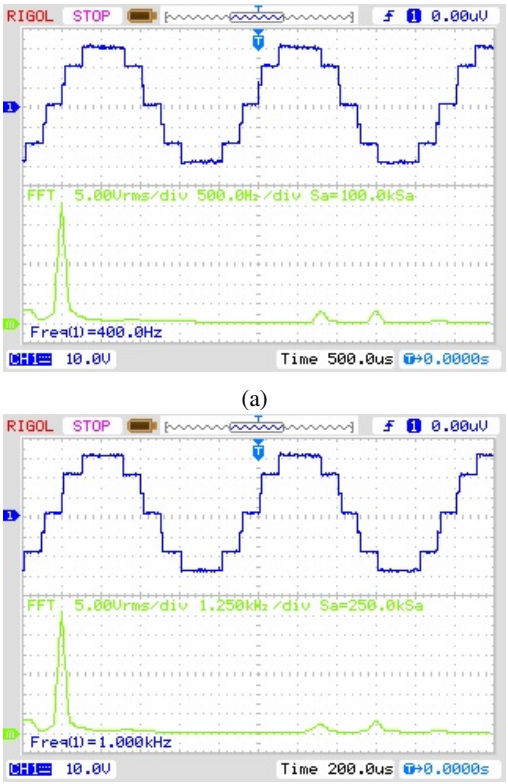
(a)

(b)

Fig. 9: Measured 1kHz output with resistive loads. Ch. 1: Output voltage, Ch. 2: Output Current. (a) 37 W (b) 255 W

TMS320F28335 controller to implement SHE for the proposed SCMLI. Table VI shows the values of θ_1, θ_2 and θ_3 at different modulation indices. Since the output voltage of the SCMLI is a function of the modulation index (8), the modulation index can be adjusted real time to realize the required magnitude of output voltage. To realize this, a look table with values of switching angles for various M_I should be programmed into the DSP. The required modulation index can be chosen depending on whether the output voltage needs to be stepped up or down, the information of which is obtained from the feedback.

Simulation and experimental results of seven level output voltage and current, and SC voltage and current waveforms



(a)

(b)

Fig. 10: Measured FFT with resistive loads. Ch. 1: Output voltage (use 2x multiplier), Ch. M: FFT plot. (a) 400 Hz (b) 1000 Hz

operating at M_I = 0.84 with output frequency of 400 Hz are shown in Fig. 7 and Fig. 8 respectively. Fig. 9 (a) and (b) show the 7 level staircase output voltage and current at 1 kHz working at 37 W and 255 W respectively. It can be observed that the voltage drop increases at higher power operation. If the voltage drop is severe, the output voltage is no longer close to the desired staircase waveform. This increases the line harmonics. Voltage drop at higher power levels can be reduced either by increasing the value of SC or by increasing the operating frequency.

FFT analysis of SCMLI's output voltage waveforms operating at 400 Hz and 1 kHz distribution frequencies is shown in Fig. 10 (a) and (b) respectively and tabulated in Table IV. Employing SHE, 5^{th} and 7^{th} harmonics are minimized. Small magnitudes of 3^{rd}, 9^{th} and 11^{th} harmonic still exist. If an optimum value of capacitor is not chosen for a given power level and output frequency, the harmonic content in the output waveform will increase and cause several undesired effects. Better modulation schemes can also be adopted to optimize the switched-capacitor size for a given frequency.

Fig. 11 shows the plot of efficiency versus output power at different distribution frequencies. It is observed that as the frequency increases, the efficiency of the inverter increases. This can be explained from Fig. 12, which shows the variation in SC ripple voltage with frequency and output power. For a given power level, increasing the distribution frequency reduces the SC ripple voltage, thereby improving the operating

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

TABLE VI: SHE Switching angles for different modulation indices

M_I	θ_1	θ_2	θ_3
0.5	39.4°	56.25°	80.1°
0.6	11.8°	41.7°	85.7°
0.7	18.3°	44.1°	64.4°
0.84	15.6°	18.7°	52.4°
0.92	7.98°	15.3°	36.4°

efficiency. To further mitigate switching losses, a resonant front-end SC converter can be designed by adding a series inductor to realize zero current switching. However, this will increase the voltage stress on the devices employed.

Fig. 13 shows the output waveforms with inductive load. An inductor is connected in series with a variable resistor as the load. For the experiment, L = 1 mH, R = 58 Ω was used. The value of the phase angle is equal to 15.15°. It can be observed that the output voltage is similar to that with R load. However, the current waveform is more sinusoidal. This waveform validates that the proposed SCMLI can work as a HF source to power inductive loads with a small phase difference and is mostly applicable in high power factor applications or supplying active power to microgrids from renewable energy farms. However, Table VI implies that at low modulation indices a larger inductive load can be supported.

VIII. Discussion

Consider an example of an electric golf-car (classified under small car). If input voltage from the sources are below 48 V, it falls under the category of safe operating voltages. This in turn mitigates the overall cost as it eliminates the need to install expensive high voltage protective features. Therefore, the primary battery is usually rated below 48 V DC. Additionally, modern golf-cars equipped with solar panels charge the auxiliary battery to a lower value of around 20 V. Another example is the hybrid electric car powered by Li-ion batteries and super-capacitors. Since the nominal voltage of Li-ion battery is 3.7 V and that of super-capacitor is 2.7 V, the voltage levels of these series connected energy storage devices are bound to differ.

Both these respective pairs of voltage sources can be used as inputs to generate a high frequency AC distribution line. The high frequency AC power is rectified before driving the DC motor and other loads. In the proposed SCMLI, if the difference between the two input voltage sources is not large enough, then the advantages diminish. However, with higher voltage levels the cost of implementation increases as there is a need to add protective features for high voltage operation. Future work includes to investigate PWM techniques to optimize THD levels for unequal voltage steps.

IX. Conclusion

A novel SCMLI topology for HFAC PDS has been proposed in this paper. The topology is applicable where unequal DC input sources are at disposal. Such scenarios are common in large renewable energy farms and electric vehicle networks. It

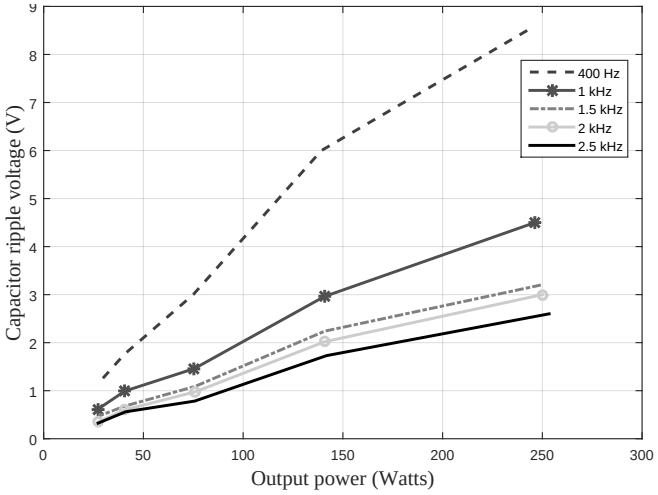


Fig. 11: Measured efficiency versus output power at different output frequencies

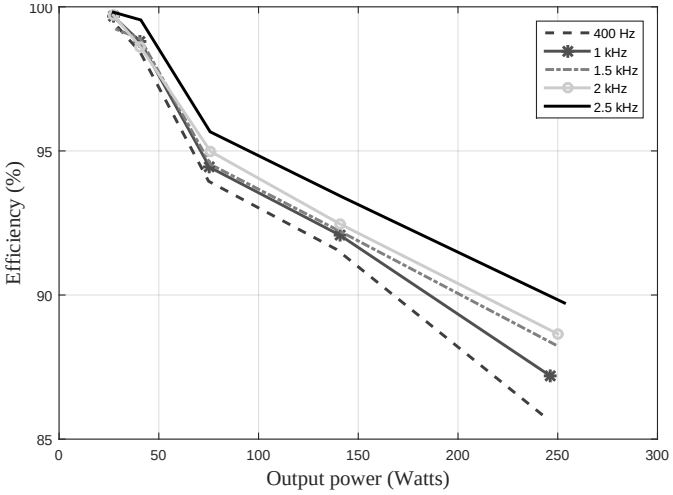


Fig. 12: Measured peak to peak capacitor ripple voltage versus output power at different output frequencies

is more convenient to employ multiple DC sources as input to a single inverter than to employ several inverters in parallel with their respective solitary DC input sources. This topology does not stack up the voltage sources in series and therefore does not require voltage balancing circuits. Since the switched-capacitors employed copy the input voltage every cycle, the problem of voltage balancing has also been eliminated. The harmonic content in the waveform is analyzed and is found to be minimum. The proposed topology obtains higher number of voltage levels compared to several existing topologies. This paper utilizes the proposed topology for high frequency AC distribution. However, the same topology can be employed for 50 Hz / 60 Hz distribution by employing a larger switched-capacitor. It is shown that the number of output voltage levels exponentially increase with increase in the employed input voltage sources and SCs. In the hardware results, it is shown that the 5^{th} and 7^{th} harmonics are minimized to very low

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

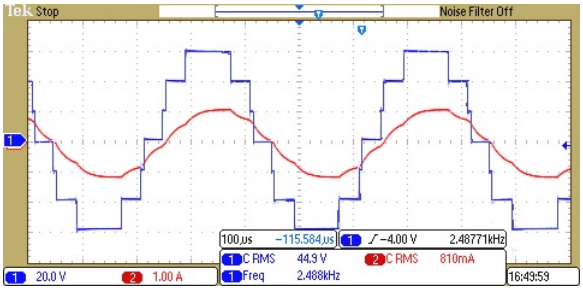


Fig. 13: Measured 2.5 kHz waveforms with inductive load. Ch. 1 : Output voltage, Ch. 2: Output Current

value of 1V each. Results at different distribution frequencies and power levels are presented.

ACKNOWLEDGMENT

This work was supported by The Hong Kong Polytechnic University under Project Number GHP/057/14AP. The authors wish to acknowledge the support provided by the members of the Power Electronics Research Centre (PERC), Department of Electrical Engineering, The Hong Kong Polytechnic University.

REFERENCES

[1] Patel, Mukund R.,"High-Power High-Voltage Systems", *Spacecraft Power Systems*, CRC press, 2004, ch. 22, sec. 22.7, pp. 539-543.

[2] Luk, Patrick Chi-Kwong, and Andy Seng Yim Ng. "High Frequency AC Power Distribution Platforms." Power Electronics in Smart Electrical Energy Networks. Springer London, 2008. pp. 175-201.

[3] Z. Ye, P. K. Jain and P. C. Sen, "A Two-Stage Resonant Inverter With Control of the Phase Angle and Magnitude of the Output Voltage," in IEEE Trans. Ind. Electron., vol. 54, no. 5, pp. 2797-2812, Oct. 2007.

[4] J. A. Sabate, M. M. Jovanovic, F. C. Lee and R. T. Gean, "Analysis and design-optimization of LCC resonant inverter for high-frequency AC distributed power system," in IEEE Trans. Ind. Electron., vol. 42, no. 1, pp. 63-71, Feb 1995.

[5] *Status of 20 kHz Space Station Power Distribution Technology*, NASA Publication, TM 100781.

[6] F. S. Tsai and F. C. Y. Lee, "High-frequency AC power distribution in Space Station," in IEEE Transactions on Aerospace and Electronic Systems, vol. 26, no. 2, pp. 239-253, Mar 1990.

[7] P. Jain, et al.,"A Review of High-Frequency Power Distribution Systems: For Space, Telecommunication, and Computer Applications," in IEEE Trans. Power Electron., vol. 29, no. 8, pp. 3852-3863, Aug. 2014.

[8] C. C. Antaloae, J. Marco and N. D. Vaughan, "Feasibility of High-Frequency Alternating Current Power for Motor Auxiliary Loads in Vehicles," in IEEE Trans. Vehicular Technology, vol. 60, no. 2, pp. 390-405, Feb. 2011.

[9] M. A. Masrur, D. S. Sitar and V. A. Sankaran, "Can an AC (alternating current) electrical system replace the present DC system in the automobile? An investigative feasibility study. II. Comparison and tradeoffs," in IEEE Trans. Vehicular Technology, vol. 47, no. 3, pp. 1081-1086, Aug 1998.

[10] S. Raghu Raman, et. al, "High frequency AC auxiliary power source for future vehicles", 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, 2015, pp. 1-6.

[11] B. K. Bose, Min-Huei Kin and M. D. Kankam, "High frequency AC vs. DC distribution system for next generation hybrid electric vehicle," Industrial Electronics, Control, and Instrumentation, Proceedings of the 1996 IEEE IECON 22nd International Conference on, Taipei, 1996, pp. 706-712 vol.2.

[12] S. Chakraborty, M. D. Weiss and M. G. Simoes, "Distributed Intelligent Energy Management System for a Single-Phase High-Frequency AC Microgrid," in IEEE Trans. Ind. Electron., vol. 54, no. 1, pp. 97-109, Feb. 2007.

[13] H. Wen, W. Xiao and Z. Lu, "Current-Fed High-Frequency AC Distributed Power System for Medium-High-Voltage Gate Driving Applications," in IEEE Trans. Ind. Electron., vol. 60, no. 9, pp. 3736-3751, Sept. 2013.

[14] S. Kouro et al., "Recent Advances and Industrial Applications of Multilevel Converters," in IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553-2580, Aug. 2010.

[15] J. Rodriguez, Jih-Sheng Lai and Fang Zheng Peng, "Multilevel inverters: a survey of topologies, controls, and applications," in IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724-738, Aug 2002.

[16] Z. Li, P. Wang, Y. Li and F. Gao, "A Novel Single-Phase Five-Level Inverter With Coupled Inductors," in IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2716-2725, June 2012.

[17] J. Salmon, A. M. Knight and J. Ewanchuk, "Single-Phase Multilevel PWM Inverter Topologies Using Coupled Inductors," in IEEE Trans. Power Electron., vol. 24, no. 5, pp. 1259-1266, May 2009.

[18] E. Najafi and A. H. M. Yatim, "Design and Implementation of a New Multilevel Inverter Topology," in IEEE Trans. Ind. Electron., vol. 59, no. 11, pp. 4148-4154, Nov. 2012.

[19] E. Zamiri, et. al,, "A New Cascaded Switched-Capacitor Multilevel Inverter Based on Improved Series-Parallel Conversion With Less Number of Components," in IEEE Trans. Ind. Electron., vol. 63, no. 6, pp. 3582-3594, June 2016.

[20] R. Barzegarkhoo, et. al, "Generalized Structure for a Single Phase Switched-Capacitor Multilevel Inverter Using a New Multiple DC Link Producer With Reduced Number of Switches" in IEEE Trans. Power Electron., vol. 31, no. 8, pp. 5604-5617, Aug. 2016.

[21] J. Liu, K. W. E. Cheng and Y. Ye, "A Cascaded Multilevel Inverter Based on Switched-Capacitor for High-Frequency AC Power Distribution System," in IEEE Trans. Power Electron., vol. 29, no. 8, pp. 4219-4230, Aug. 2014.

[22] Y. Ye, et. al., "A Step-Up Switched-Capacitor Multilevel Inverter With Self-Voltage Balancing," in IEEE Trans. Ind. Electron., vol. 61, no. 12, pp. 6672-6680, Dec. 2014.

[23] E. Babaei and S. S. Gowgani, "Hybrid Multilevel Inverter Using Switched Capacitor Units," in IEEE Trans. Ind. Electron., vol. 61, no. 9, pp. 4614-4621, Sept. 2014.

[24] A. Tsunoda, Y. Hinago and H. Koizumi, "Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion," in IEEE Trans. Ind. Electron., vol. 61, no. 8, pp. 4011-4021, Aug. 2014.

[25] Y. Hinago and H. Koizumi, "A Switched-Capacitor Inverter Using Series/Parallel Conversion With Inductive Load," in IEEE Trans. Ind. Electron., vol. 59, no. 2, pp. 878-887, Feb. 2012.

[26] J. Liu; J. Wu; J. Zeng; H. Guo, "A Novel Nine-Level Inverter with One Voltage Source and Reduced Voltage Stress as High Frequency AC Power Source," in IEEE Trans on Power Electron.

[27] Eguchi, Kei, Ya Nan Zhang, Kuniaki Fujimoto, and Hirofumi Sasaki. "Design and Analysis of a Fibonacci Switched-Capacitor DC-AC Inverter." In Applied Mechanics and Materials, vol. 666, pp. 82-86. Trans Tech Publications, 2014.

[28] M. S. W. Chan and K. T. Chau, "A new switched-capacitor boost multilevel inverter using partial charging," IEEE Trans. Circuits Syst.II: Exp. Briefs, vol. 54, no. 12, pp. 1145?1149, Dec. 2007.

[29] S. Raghu Raman et al., "Switched-Capacitor Multilevel Inverters for High Frequency AC Microgrids", 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.

[30] S. Raghu Raman et al., "A Seven Level Switched Capacitor Multilevel Inverter with Asymmetric Input Sources for Microgrids", The 20th International Conference on Electrical Machines and Systems (ICEMS), Sydney, NSW, Australia, Aug. 2017

[31] Y. C. Fong et al., "A Hybrid Multilevel Inverter Employing Series-parallel Switched-capacitor Unit," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, 2017.

[32] J. Liu, K. W. E. Cheng and J. Zeng, "A Unified Phase-Shift Modulation for Optimized Synchronization of Parallel Resonant Inverters in High Frequency Power System," in IEEE Trans. Ind. Electron., vol. 61, no. 7, pp. 3232-3247, July 2014.

[33] J. R. Wells, B. M. Nee, P. L. Chapman and P. T. Krein, "Selective harmonic control: a general problem formulation and selected solutions," in IEEE Trans. Power Electron., vol. 20, no. 6, pp. 1337-1345, Nov. 2005.

[34] Haaf Peter, and Jon Harper. "Understanding diode reverse recovery and its effect on switching losses." 2007.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TPEL.2017.2742525, IEEE Transactions on Power Electronics

S. Raghu Raman (S'13) received the B.E. degree in Electrical and Electronics Engineering from Visvesvaraya Technological University, Belagavi, Karnataka, India in June 2012. He interned with the Dept. of Aerospace Engineering, Indian Institute of Science (IISc), Bengaluru, Karnataka, India during summer 2010. Upon graduation, he joined the Power Electronics Group, Dept. of Electrical Engineering, IISc as a research assistant. In Feb. 2014, he joined Power Electronics Research Centre, Dept. of Electrical Engineering, The Hong Kong Polytechnic University as a research assistant and has been working toward the Ph.D. degree.
His research interests include design and control power converters, battery, super-capacitors and fuel cell based systems, electric vehicle and renewable energy technologies.

K. W. E. Cheng (M'90-SM'06) received the B.Sc. and Ph.D. degrees from the University of Bath, Bath, U.K., in 1987 and 1990, respectively. Before joining the Hong Kong Polytechnic University, Kowloon, Hong Kong, in 1997, he was with Lucas Aerospace, U.K., as a Principal Engineer, where he led a number of power electronics projects. He has authored / co-authored more than 250 papers and 7 books. He is currently a Professor at the dept. of Electrical Engineering and Director of Power Electronics Research Centre, Hong Kong Polytechnic University.
Dr. Cheng's research interests include all aspects of power electronics, motor drives, electromagnetic interference, electric vehicle, battery management, and energy saving. He received the IEE Sebastian Z De Ferranti Premium Award in 1995, the Outstanding Consultancy Award in 2000, the Faculty Merit Award for best teaching in 2003 from the Hong Kong Polytechnic University, the Faculty of Engineering Industrial and Engineering Services Grant Achievement Award in 2006, the Brussels Innova Energy Gold Medal with Mention in 2007, the Consumer Product Design Award in 2008, the Electric Vehicle Team Merit Award of the Faculty in 2009, Geneva Invention Expo Silver Medal in 2011, Eco Star Award in 2012, Gold Prize for the design and development of body integrated super-capacitor panels for electric vehicles, at Seoul International Invention (2015) and iCAN 2016 for contribution in active suspension for vehicles.

Yuanmao Ye (M'16) received the B.Sc. degree in electrical engineering from University of Jinan, Jinan, China, in 2007, the M.Sc. degree in control theory and control engineering from South China University of Technology, Guangzhou, China, in 2010, and the Ph.D. degree from the Hong Kong Polytechnic University, Hong Kong, in 2016. From September 2010 to January 2014, he was with the Department of Electrical Engineering, Hong Kong Polytechnic University, as a Research Assistant.
He is currently a full Professor in School of Automation, Guangdong University of Technology. His research interests include various dc-dc power converters, switched-capacitor technique and its applications, multilevel inverters, power conversion and energy management for smart-grids, protection and control techniques for DC distribution, wireless charging technique for EVs.